A 2.488 Gb/s 1:4/1:16 DEMULTIPLEXER: AN EXPERIENCE ON THE DESIGN OF HIGH-SPEED DIGITAL GaAs ICs

Fatima S. Correra and Taufik Abrão

Laboratório de Microeletrônica
Escola Politécnica - Universidade de São Paulo
Av. Prof. Luciano Gualberto, tr. 3, no. 158
CEP 05508-900 São Paulo, SP - Brazil
Telephone: 818 52 55 Fax: 818 55 85
e-mail addresses: fscorrer@lme.poli.usp.br tabrao@lme.poli.usp.br

Abstract

This paper reports an experience on the design of high-speed digital GaAs ICs, emphasizing the issues on circuit architecture, layout, fabrication and characterization at Gb/s rates. A 1:4/1:16 demultiplexer IC has been designed to operate up to 2.5 Gb/s. The demultiplexer employs a tree type architecture based on 1:2 demux blocks using Tristage flip-flops, that allows high-speed performance with low power dissipation. A new skip circuit without re-timing at clock rate was proposed and integrated to the demultiplexer for frame alignment purposes. The IC has been fabricated employing 1 µm MESFET SCFL standard cells from a commercially available foundry service. The proposed skip circuit demonstrated its effectiveness and the IC operated successfully either as a 1:4 or a 1:16 demultiplexer up to 2.5 Gb/s with power dissipation of 1 W. This IC is applicable for signal processing on SONET STS-12/48 optical communication systems.

1. INTRODUCTION

High-speed digital circuits are a key component to improve the performance of commercial computers, military electronic systems, communication systems and instrumentation. Gallium Arsenide based ICs emerged as a solution for high-speed applications, presenting low power dissipation at Gb/s operation range.

The first commercially available digital GaAs ICs operating at Gb/s rates were announced in 1983 [1] and the first GaAs IC Guide, for both digital and analog circuits, was published in 1986 [2]. Former digital GaAs ICs were based on MESFET technology, that is still the most used one up to now. The application of HEMT and HBT technologies on the design of high-speed ICs has been largely reported lately, demonstrating the potential of these emerging technologies to increase the operation bit rate of integrated circuits [3-5].

Developing high-speed digital GaAs ICs is a very challenging task in many ways, but it became more suitable with the emergence of GaAs foundry services that gave customers the access to well established GaAs process for the prototyping of their ICs. Some of the GaAs foundries offer low-cost multi-user prototyping services that are affordable for research and development groups, as well as for academic activities.
Optical communication systems with high data capacity are a large application area for high-speed digital GaAs ICs. The development of these high data capacity systems was stimulated by the increase in the communication needs over all the world in the last years. Optical communication systems transmit digital data at Gb/s rates and employ high-speed digital ICs for signal processing purposes, as laser drivers, crosspoint switches, multiplexers, demultiplexers, phase shifters, decision circuits and clock recovery circuits.

In this paper we present design considerations and experimental results of a 2.5 Gb/s demultiplexer IC with an integrated skip circuit. This IC was developed at University of São Paulo in cooperation with CPqD-Telebrás, Brazilian Telecommunication Agency R&D Center (contract Telebrás-USP JDPqD 516/93). The demultiplexer works either as a 622 Mb/s 4-bit demux or as a 2.488 Gb/s 16-bit demux, and is intended for use in both optical communication systems SONET STS-12 and STS-48 systems. A new skip circuit topology without re-timing at clock rate was proposed and integrated to the demultiplexer for frame alignment purposes.

This circuit was constructed using a 1µm MESFET foundry technology commercially available and, from the authors acknowledgment, it represents the first result of Brazilian engineering on the design of GaAs integrated circuits operating at Gb/s rates.

In the following sections of this paper we present the design considerations and experimental results of a demultiplexer IC with an integrated skip circuit. Relevant topics on high-speed digital ICs development are discussed, covering issues on foundry selection, circuit topology, layout and electrical characterization at Gb/s rates.

II. FOUNDRY SELECTION

One of the first steps on the development of the circuit is the selection of a GaAs foundry for prototyping the digital IC. There are many important aspects to be considered when selecting a foundry:

- the maximum toggle frequency of the fabrication process offered by the foundry;

- the availability of accurate foundry models to represent the behavior of both circuit elements, as transistors, resistors, standard cells, and layout parasitic elements up to several Gigahertz;

- the availability of a multi-user option that allows low cost prototyping of the IC at research and development stages and a professional prototyping service for high volume production in the case the IC become commercial.

Low cost multi-user prototyping services for digital GaAs ICs are offered by a limited number of foundries when compared to foundries for Silicon ICs. Technologies based on GaAs MESFETs are available from TriQuint Semiconductor, Inc, Vitesse and Philips Microwave Limeil (PML). The foundries TriQuint and Philips Limeil Microwave organize their own multi-user prototyping runs. The services of Vitesse may be accessed through Circuits Multi Projects, CMP, that prepares multi-user runs for this foundry.
Table 1 shows information on MESFET technologies offered by TriQuint, Vitesse and PML for customers of multi-user runs. Customers that design ICs at transistor level can access technologies based on MESFETs with gate lengths ranging from 0.6 to 1 µm. The designers have also the option of using elements from standard cells libraries on their circuits. In such a case the available technologies are more restricted. TriQuint offers 1 µm MESFET based standard cell library, employing Source Coupled FET Logic (SCFL) elements, with guaranteed operation up to 2 Gb/s. Customers of multi-user runs can access standard cells from a Direct Coupled FET Logic (DCFL) library from Vitesse, that operate up to 1 Gb/s. Philips Microwave Limeil offers both SCFL and DCFL libraries for their customers.

**Table 1 - General characteristics of TriQuint, Vitesse and PML process for digital ICs**

<table>
<thead>
<tr>
<th>Foundry:</th>
<th>TriQuint</th>
<th>Vitesse</th>
<th>PML</th>
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<tr>
<td>MESFET gate length</td>
<td>1 µm / 0.7 µm</td>
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<td>Enhanced MESFETs</td>
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<tr>
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<tr>
<td>Maximum toggle frequency</td>
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<td>3 Gb/s / ---</td>
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<td>Standard Cell Library</td>
<td>SCFL (2 Gb/s)</td>
<td>DCFL (1Gb/s)</td>
<td>SCFL / DCFL</td>
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The demultiplexer presented in this paper was fabricated using the standard cell library QLSI from TriQuint, based on 1 µm MESFET SCFL elements. The SCFL logic family has superior performance over other GaAs logic families as DCFL, when considering high-speed operation. An other advantage of SCFL logic family is the small dependence of the logic ports operation on \( V_{th} \), the MESFET threshold voltage. That is an very important advantage since \( V_{th} \) is very sensitive to process variation on the construction of MESFETs. As an example it was verified that SCFL logic ports designed for nominal \( V_{th} = -0.1 \) V could operate properly for \(-0.6 \, V \leq V_{th} \leq +0.4 \, V\) [6]. It is interesting to remark that DCFL logic gates are less power consuming than SCFL ones, being advantageous for the implementation VLSI circuits.

Figure 1 presents the basic structure of a AND/NAND gate implemented using SCFL logic family. As can be seen in this figure, the SCFL logic family operates at current mode logic, as the ECL logic family using Silicon bipolar transistors. The input signals are applied to differential pairs of MESFETs, what makes the circuit operation less sensitive to variation on the \( V_{th} \) of the transistors. The differential output signals of the logic gate are taken from two output buffers. It is interesting to remark that SCFL is a multi-level logic: the output buffers include level shifting diodes, so that the logic output signals are available on different voltage levels. The circuit presented in figure 1 has tree output levels, but up to four output levels should be obtained at SCFL gates without degrading their intrinsic delay.

The QLSI standard cell library contains core cells to perform logic operations and input/output cells that convert SCFL logic levels to ECL, CMOS and TTL logic levels and vice versa. Both core cells and I/O cells are available in multiple power families, in order to facilitate the optimization of each circuit design for high-speed operation with power consume.

The maximum toggle rate guaranteed by the foundry for the elements of QLSI standard cell library is 2 Gb/s on the worst case of process, temperature and power supply variations.
Circuits operating at higher bit rates can be designed with elements of this library, but a decrease in the fabrication yield should be expected.

In the design of the demultiplexer we aimed circuit operation up to 2.488 Gb/s, so that special attention was taken on the circuit design to overcome the frequency limitation of QLSI standard cell library.

III. CIRCUIT ARCHITECTURE

As explained previously, the circuit was designed using elements from the QLSI### standard cell library from TriQuint Semiconductor, Inc. This library is based on 1 ###m FET SCFL logic gates and is specified to operate up to 2.0 Gb/s. To overcome this bit rate limitation the following procedures were adopted [7]:

a) a tree type demultiplexer topology was used that minimizes the number of elements operating at clock rate;

b) a bypass to the first clock divider circuit was provides, so that the IC could be driven by clock/2 instead of the clock signal at high bit rates;

c) a new skip circuit without retiming at clock rate was proposed.

In order to define the demultiplexer architechture tree type and shift register demultiplexer topologies were compared in terms of power consume, area and high speed performance. The tree type topology presented the best overall performance and was adopted for the demultiplexer. The authors intend to present a detailed comparison of available demultiplexer architectures in a future publication.

As shown in figure 2, the demultiplexer employs a four level tree type circuit topology [8] using 1:2 demux blocks composed by Tristage flip-flops [9] and D flip-flops. For 1:16 demux operation mode all data outputs D1 to D16 are enabled and the clock/16 signal is present at the output clock port. When the 1:4 demux operation mode is selected, the outputs from the second demultiplexation level are driven to the data outputs D4, D8, D12 and D16 through the selectors S1 to S4. The remaining data outputs are disabled and the clock/4 signal is selected as the output clock through selector S5. A delay was introduced at the input data signal path in order to guarantee it to be sampled at the proper phase by the first 1:2 demux block. This delay was optimized envisaging the circuit operation at 2.5 Gb/s and combines the delay of logical gates and the physical delay due to the layout parasitic capacitance from metal interconnections.

The time diagram presented at figure 3 illustrate the operation of the demultiplexer circuit in both modes 1:4 demux and 1:16 demux. As shown in this time chart, when the demultiplexer operates at 1:4 demux mode, the remaining outputs are disabled, keeping constant logic values.
Figure 4 presents the topology of the proposed skip circuit. This circuit was obtained modifying the skip circuit presented at reference [10] and was especially developed for improved performance when the demultiplexer operates at high speed. Retiming steps at clock rate were avoid and all the logic gates on the skip circuit operate at clock/2 rate, except the clock divider circuit that is driven by the clock signal. This way, the clock divider circuit is the element that limits the high speed operation of the skip circuit. This limitation can become critical when the intrinsic delay time of the standard cells increase due to variation on the circuit fabrication process. To overcome this limitation, a bypass to the clock divider circuit was provided that allows the skip circuit to be driven by clock/2 instead of clock signal at high bit rates, increasing the circuit fabrication yield.

A detailed time diagram of the proposed skip circuit is shown in figure 5. The skip circuit is sensitive to transitions of the asynchronous control signal (SKP) applied to its input. The skip control signal is synchronized to clock/2 using a D flip-flop and actuates the selector SELM, connecting either clock/2 or its complement (ck/2 or nck/2) to the selector output. The relative phase between clock/2 and the skip control signal at the selector inputs was carefully adjusted during the circuit design. As a result, half cycle of the signal at the selector output (Ck/2_skp) is skipped with minimum spike effects when the skip control is actuated.

IV. SELECTION OF STANDARD CELLS

Once the demultiplexer architecture is chosen, it is necessary to select the standard cells to be used on the circuit implementation. In this step we have to consider the operation bit rate of the standard cell, its interaction with other circuit elements and also its power consume. The main considerations on the selection of the standard cells are:

a) The maximum toggle frequency of the standard cell, F_{max}, should be greater than the operation bit rate of the cell in the circuit.

The maximum toggle frequency depends on the total capacitive loading of the standard cell, C_{load}, presented in equation 1:

\[
C_{\text{load}} = C_{\text{fan-out}} + C_{\text{wire}} \quad (1)
\]

where:

\(C_{\text{fan-out}}\): is the capacitance due to the fan-out

\(C_{\text{wire}}\): is the wiring capacitance

The fan-out capacitance is the sum of the input capacitance, \(C_{\text{in}}\), of the standard cells connected to the output node:

\[
C_{\text{fan-out}} = \#\#\ C_{\text{in}} \quad (2)
\]
The wiring capacitance, \( C_{\text{wire}} \), comes from metallic interconnects among standard cells and will result in extra loading at the cell outputs. Wiring capacitance should be carefully accounted on the high-speed ICs. In technologies based on GaAs MESFETs, \( C_{\text{wire}} \) has the same order of magnitude as \( C_{\text{in}} \) and it has to be minimized during the circuit layouting. The wiring capacitance per unit length depends on the IC fabrication process. The TriQuint’s QED/A technology used to fabricate the demultiplexer employs a two layer metallization with the following characteristics:

- Capacitance per unit length: 0.15 fF/\( \mu \text{m} \) for metal 1 layer, for width = 2 \( \mu \text{m} \)
- 0.07 fF/\( \mu \text{m} \) for metal 2 layer, for width = 3 \( \mu \text{m} \)

In order to account for wiring capacitance before circuit layouting, the following empirical formula is suggested by TriQuint [11] for users of its QED/A process:

\[
C_{\text{wire}} = C_{\text{FO}} (F_O + 1)^{1.1} \tag{3}
\]

where:

- \( F_O \): is the number of ports connect the node
- \( C_{\text{FO}} \): ranges from 25 fF to 35 fF depends on the number of standard cells integrated in the circuit

Once the output loading of the standard cell is known, the maximum toggle frequency for the worst case of process and temperature variation can be calculated from equations 4a and 4b:

\[
F_{\text{max}} = [2t_{\text{pw}}]^{-1} \tag{4a}
\]

\[
t_{\text{pw}} = 1.5 t_{\text{tpd}} + 2.6 \times \text{Loading Delay} \times C_{\text{load}} \tag{4b}
\]

where:

- \( t_{\text{pw}} \): pulse width
- \( t_{\text{tpd}} \): base delay of the standard cell
- \( \text{Loading Delay} \): loading delay per unit capacitance

b) The dynamic switching energy, \( P_{\text{diss}} \times t_{\text{tpd}} \), should be minimized on the implementation of LSI high-speed digital ICs in order to obtain the aimed high-speed operation with minimum power consume. This is obtained using the lower powered standard cell that satisfies the condition presented in the previous item.

It is interesting to remark that standard cells with lower power consume have lower input capacitance, \( C_{\text{in}} \), representing a lighter load for the nodes where they are connected, what is important for high-speed operation.
c) The maximum clock fan-out should be considered when selecting standard cells to implement high-speed digital ICs. Usually, a single gate drives many clock inputs and clock signal edges are slowed down due to this high fan-out. This may be disastrous for the master slave flip-flops where the slave must latch before the master becomes transparent.

When implementing a circuit with standard cells QLSI library, the load delay due to fan-out and wiring should not exceed 300 ps for any gate driving clock, set or reset inputs, as stated by equation 5:

\[
\text{Load Delay} = 2.6 \cdot \text{Loading Delay} \cdot C_{\text{load}} \leq 300 \text{ ps} \quad (5)
\]

e) As shown in figure 1, SCFL standard cells have multi-level inputs and outputs due to the use of level shifting diodes. Only inputs and outputs operating with the same voltage levels can be interconnected due to compatibility reasons. Inputs at different levels will have different delays to the output \( t_{\text{pd}} \) that have to be correctly accounted when evaluating the maximum toggle frequency using equation 4.

V. CIRCUIT SIMULATION AND LAYOUT CONSIDERATIONS

The criteria presented on item IV were used to select the standard cells to be used on the implementation of the demultiplexer and skip circuits. The circuit performance was then simulated and optimized using the logic simulator from GDT version 5.2. First simulations were performed considering the characteristics of the standard cells and the wiring capacitance estimated from equation 3.

These simulations were performed before the circuit layouting and demonstrated proper operation of the circuit up to 2.5 Gb/s. Other important results from these simulations were the following layout requirements:

- the determination of critical circuit nodes where wiring capacitance should be kept to a minimum to guarantee the circuit operation at high-speed;

- the determination of the optimal length of some signal paths, to guarantee the relative phase between signals where it was relevant for proper circuit performance.

Additionally, two other very important criteria were adopted during the demultiplexer layout:

- minimization of the wiring capacitance of all the connections driving high-speed signals;

- equalization of the path length of matched pairs of connections that drive a signal and its complement.

This last consideration applies especially to SCFL standard cells that use both the signal and its complement, that care should be taken to equalize the path lengths, to minimize the delay differential due to unequal capacitive loading.
The circuit was layouted at CPqD-Telebras using Mentor V.8. Manual place and route procedures were used in order to satisfy the numerous and complex circuit layout requirements. ECL-compatible I/Os were integrated to all inputs and outputs of the circuit, resulting in a chip area of 2.5 mm X 2.5 mm.

Back-annotation tools were used to extract the wiring capacitance of the circuit layout. These parasitic capacitance were employed to perform a pos-layout simulation of the complete circuit and determine slight modifications that should be done on the layout to optimize the circuit operation. The circuit simulation is discussed in detail in item VI.

Layout versus schematic verification and design rule checking were performed before the demultiplexer circuit was send to fabrication at TriQuint Semiconductor, Inc. Figure 6 presents a microphotograph of the chip.

VI. SIMULATION RESULTS

The simulation of high-speed digital circuits is usually done at two different steps. In the first step the circuit is simulated before we have information concerning the circuit layout. However, the wiring capacitance that come from the metallic interconnects can not be neglected at high-speed and has to be estimated from an appropriate formula, as the one presented at equation 3. This preliminary simulation allow the designer to check the functionality of the circuit architecture and to optimize the overall circuit performance. The influence of the variations of fabrication process and environment temperature on the circuit performance can be evaluated on this simulation stage, to prove the possibility of constructing this circuit with an acceptable fabrication yield.

Once the desired results are obtained from the first simulation stage, circuit layout can start. After a preliminary circuit layout is done, a back-annotation is performed to extract the wiring capacitance and the pos-layout simulation can be performed. On this second simulation step allows the designer to check the circuit performance and to do any needed change on the circuit layout to improve the circuit operation at high-speed.

In both preliminary and pos-layout simulations it is necessary to developed test vectors to represent signals applied to the circuit inputs. The test vector should be as complete as possible in order to simulate all the possibilities of input signal combinations. When we are simulating digital circuits with low and medium complexity, as in the case of demultiplexers, it is possible to generate a long test vector that allows an exhaustive simulation of the circuit. Long test vectors are then generated to test the circuit functionality.

A complete simulation of all the functions of the demultiplexer was done using a long test vector to simulate all the combinations of the following items:

- circuit operation as 1:4 demux and a 1:16 demux;
- the actuation of the skip circuit on both 1:4 demux and a 1:16 demux operation modes;
- relative phase between input data and input clock signals deviating up to 20% from the nominal value;

- circuit operation when the standard cell parameters range from 0.7 to 1.5 times their nominal values due to temperature and process variation.

In order to create a long test vector for simulation of the demultiplexer, an ideal pseudo-random generator was implemented in the same file as the circuit to be simulated. The pseudo-random generator topology and its connection to the demultiplexer circuit is shown in figure 7.

The pseudo-random generator employs an $n$ (4 or 16) bit shifter register using D type flip-flops operating at the same input clock rate as the demultiplexer circuit. As shown in figure 7, some or all outputs of the shifter register drive a XNOR gate, and the resulting signal is feedback to the data input of the shift register, generating a pseudo-random sequence on the its outputs 1 to $n$. The outputs 1 to $n$ of the shifter register are retimed by the signal clock/$n$ through a bench of latch’s, generating the vector of signals [d1m, d2m ....d16m]. This same signals are present at the q output of the shifter register but multiplexed on time, consisting the input data driving the demultiplexer under simulation. The proper operation of the demultiplexer can be checked by means of a simple comparison between the demultiplexer output vector [d1, d2, d3....d16] and the signal vector [d1m, d2m, ...d16m].

The phase shifters $\Delta \Phi$ inserted between the pseudo-random generator and the demultiplexer allows to adjust the relative phase between data and clock inputs of the circuit under simulation.

The simulation file containing the pseudo-random generator and the demultiplexer was used to perform a pos-layout simulation of the demultiplexer and skip circuits considering a relative phase of 180° 20% between the input data and clock signals. The standard cell parameters were varied from 70% to 150% their nominal values to simulate the circuit behavior under process and temperature variation. The simulation results demonstrated the required circuit performance over all the simulated range. However, at 2.5 Gb/s an external delay should be added to the input data path when the standard cell parameters deviate more than -8%/+23% from nominal values.

VII. EXPERIMENTAL RESULTS

The characterization of high-speed circuits involves measurements at DC, at low-speed rates - usually tens of Mb/s, and at high-speed rates that can reach the Gb/s band. The parameters to be measured depend on the function performed by the circuit. In the case of the demultiplexer the main parameters that characterize the circuit are:

**DC measurements:**

- power consume

**Low-speed measurements:**
- circuit functionality at low-speed, including operation of clock divider circuit; 1:4 and 1:16 demux and actuation of the skip circuit.

- the range of voltage values associated to of the logic levels “0” and “1”.

**High-speed measurements:**

- electrical characteristics of the signal wave forms, as voltage levels, rise and fall times;

- circuit functionality at high-speed, including the measurement of maximum operation frequency of the demultiplexer circuit and the relative phase between output clock and output data signals;

- Phase margin and bit error rate (BER) of the demultiplexer circuit.

All these measurements have to be done at nominal environment temperature, bias supply voltage and relative phase between clock input and data input signals, as well as in the complete variation ranges specified for these parameters.

Two important issues on high-speed circuit characterization are measurement setups and test fixtures for operation at Gb/s. A first remark on the subject is that all parasitic capacitance and inductance usually present on test fixtures and measurement setups should be minimized. These parasitic elements, that are negligible at low frequencies, will probably mask the circuit behavior at the Gigahertz band if they aren’t carefully reduced.

The second point to be considered is the distributed behavior of metallic tracks and cables used to connect the circuit to the measurement instrumentation. At Gigahertz band these elements are transmission lines that carry the digital signals and have to be matched to the internal impedance of the measurement equipment used. This have to be done in order to assure proper power transfer from signal generators to the inputs of the circuit and from the circuit outputs to the measurement equipment. Signal generators, oscilloscopes, BER meters and other equipment working at Gb/s usually have input impedance of 50 Ohms. So, the metallic tracks that carry high-speed signals on the test fixture have to be designed as 50 Ohms microstrip lines. The connections from the test fixture to the measurement equipment employ 50 Ohms coaxial cables and high frequency connectors as SMA and APC3.5 standards.

Figure 8 presents the measurement setup used to characterize the 2.488 Gb/s demultiplexer. The setup employs a pattern generator that drives the inputs of the demultiplexer. A digital oscilloscope allows the measurement of the circuit output signals. 50 Ohms coaxial cables connect the pattern generator and the digital oscilloscope to the circuit test fixture.

The demultiplexer IC was mounted in the multilayer ceramic package MLC68. The packaged circuit was inserted in a test fixture ETF-MLC68, that connects the package lids to controlled impedance 50 Ohm lines by a solder less mounting process. The input signal lines were terminated to -2.0 V through 50 Ohm resistors, as recommended for ECL compatible circuits. These 50 Ohm resistor were placed close to the package in order to avoid signal reflection due to impedance mismatching between the pattern generator and the demultiplexer. The IC was
biased with -5.2 V supply voltage, presenting 1.4 W of power dissipation and signal output levels compatible to ECL standards.

ECL terminators were developed to create an interface between the ECL compatible outputs of the demultiplexer circuit and the 50 Ohm instrument input. As shown in figure 9 the ECL terminator presents an input impedance of 50 Ohms to Vtt (-2 V) when its output is connected to the oscilloscope. The ECL terminator was constructed using fotolitographic technics, soft substrate and surface mounted resistors and capacitors at Laboratorio de Microeletronica, University of Sao Paulo. The ECL terminator demonstrated proper operation presenting -3 ± 0.1 dB of insertion loss and less than -25 dB of return loss up to 3 GHz.

The functionality of the demultiplexer was demonstrated by measuring the circuit performance with low speed signals (10 Mb/s clock) and high speed signals (622 Mb/s and 2.488 Gb/s clock) at room temperature. The circuit was driven by input data and clock signals with 180° of relative phase and ECL logic levels. Figure 10 shows typical input clock, output clock and output data wave forms of the IC operating as a 1:4 demultiplexer at 622 Mb/s clock, when a 1/8 signal pattern is applied to the input data port. The measured rise and fall times for the output data signal shown in the figure were 630 ps and 430 ps, respectively. The relative phase between the output clock and the output data signals was 192°.

The performance of the IC operating as a 1:16 demultiplexer at 2.488 Gb/s clock rate is presented in figures 11 and 12. Figure 11 shows the input and output clock signals wave forms, demonstrating the right operation of the clock divider circuit up to 2.488 Gb/s.

Figure 12 shows the good alignment between the output data and output clock signals when a pseudo random signal is applied to the demultiplexer data input.

The effectiveness of the skip circuit proposed in this paper was experimentally verified for the IC operating at 1:4 and 1:16 demultiplexer modes up to 2.488 Gb/s.

The demultiplexer circuit was also tested bypassing the first clock divider and driven the circuit with clock/2 instead of clock signal, and demonstrated the required performance. This operation mode may be used in the case the variation of the circuit technology made the first clock divider to fail at 2.488 Gb/s.

VIII. CONCLUSIONS

An experience on the design of high-speed digital GaAs Ics was reported, emphasizing the issues on circuit architecture, layout, fabrication and characterization at Gb/s rates. A 2.488 Gb/s demultiplexer with low power dissipation was designed to operate either as a 4-bit demux or a 16-bit demux. A skip circuit employing a new topology was integrated to the demultiplexer.

The circuit was constructed using 1 ###m MESFET SCFL standard cells from a commercially available foundry service. The demultiplexer operated up to 2.488 Gb/s with 1.4 W of power
dissipation. The experimental results demonstrated the effectiveness of the proposed skip circuit.

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REFERENCES

Figure 1.
Figure 2.
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(*) Absence of logic level transition

Figure 3.
Figure 4.

Figure 5.
Figure 6.
Figure 9.

Figure 10.
Figure 11.

![Graph showing CKOUT and Dout with a timebase of 2.00 ns/div.]

Figure 12.
FIGURE CAPTIONS

Figure 1. AND/NAND cell implemented on SCFL logic family

Figure 2. Topology of 1:4/1:16 demultiplexer.

Figure 3. Time diagram of 1:4/1:16 demultiplexer

Figure 4. Skip circuit topology.

Figure 5. Time diagram of skip circuit.

Figure 6. Microphotograph of the demultiplexer IC with skip circuit.

Figure 7. Demultiplexer simulation arrangement with ideal pseudo-random generator

Figure 8. Basic setup and test fixture for IC characterization at Gb/s rates.

Figure 9. Schematic diagram of ECL terminator

Figure 10. Input clock, output clock and output data wave forms for 1:4 demux at 622 Mb/s clock rate.

Figure 11. Input and output clock wave forms for the 1:16 demultiplexer at 2.488 Gb/s clock rate.

Figure 12. Output clock and output data wave forms for the 1:16 demultiplexer at 2.488 Gb/s clock rate.