CMOS Analog Four-Quadrant multiplier using lateral PNP Core

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Abstract
An implementation in CMOS technology of a 4-quadrant analog multiplier, whose core uses six parasitic lateral bipolar transistors is presented in this paper. Thanks to the noise characteristics of the used lateral bipolar transistors the implemented multiplier has proven to feature an improved performance with respect to THD and 1/f noise as compared to most all-MOS versions of known analog multipliers. Samples of the developed circuit were fabricated in 0.6µm CMOS technology and tested. Measurements have shown that the circuit features a bandwidth of 30MHz for 50 Ohms resistive load, THD of less than 1.0% for full-scale input and a midband equivalent noise voltage density of 300nV/√(Hz) at 100Hz.

1. Introduction
Multipliers are widely used in analog signal processing for rectification, multiplication, modulation, frequency translation, signal compression and so on. Multipliers perform non-linear operations on continuous-valued analog signals. The Gilbert Cell [1] is widely employed to implement analog four quadrant multipliers in Bipolar and MOS technology [2]. However, all-MOS implementations are more complex requiring more die area. Furthermore, problems associated with circuit complexity like distortion and noise are more susceptible to take place [3]. On the other hand, bipolar implementations using nowadays-available BICMOS process are costly. In this context, the use of parasitic bipolar transistors available in CMOS technology comes up as a possible approach to implement the proposed multiplier circuit. Several reports on literature have shown the use of the lateral bipolar transistor for implementing the more diverse circuit applications [4]. Disadvantages which contributes to reduce the emitter-collector current ratio α. Moreover, the lateral bipolar transistor is known to have low collector-base current ratio β. Therefore, the base current cannot be neglected as usual in normal bipolar devices. On the other hand, this device shows a relative low current roll-off corner, causing the device to enter in high-injection at low currents when the coefficient of the exponential function that rules the $I_C$–$V_{BE}$ relationship of the transistor departs from one. Circuits using this device can experience signal distortion if current deviation from operating point is large enough. The signal distortion can be minimized if all transistors in the circuit are operated approximately at same current levels for all signal excursions as proposed for the multiplier circuit. Fig. 1 shows the β parameter extracted for a single lateral bipolar device implemented in 0,6µm CMOS process along with the device cross-section view. Fig. 2 shows for same device the $I_C$–$V_{BE}$ relationship showing the high-injection effect.

Despite being an inferior device compared to an actual BJT, the lateral bipolar transistor available in CMOS technology can be used for specific purposes where MOS implementation is not possible. For example, in [6] a function generator is proposed using the lateral bipolar transistor achieving a non-linearity of

![Fig. 1. Current ratio β and device cross-section view.](image1)

![Fig. 2. $I_C$–$V_{BE}$ relationship showing the high injection effect](image2)
3. Basic Principle and Theory

The core multiplier is shown in Fig. 3. It features a Gilbert Multiplier Cell [6] implemented in CMOS process using six-lateral bipolar devices. To reduce signal distortion all transistors operate at high-injection condition set by the bias current source (2.1). Two MOS transconductors convert the differential input voltage $V_{in1}$ and $V_{in2}$ into differential currents that is fed to the core multiplier e.g., $I(1+x)$, $I(1-x)$, $I(1+y)$, $I(1-y)$. The differential input current is given by two complementary signals x and y around a common bias current I as indicated. Signals x and y are supposed to fluctuate between ±1. Due to the low transistor β the base current changes and so does the parameter less sensible to that transistor, causing an increase of non-linearity in circuit operation. Higher bias current make the parameter more sensible to current changes. Likewise, moderate variations around the operating point brings about the same effect, giving rise to a non-linearity operation of less than 1%, as will be shown in Experimental Results Session. For design purposes, an average β based on the operating point can be used for calculating the overall gain of the circuit.

The differential voltage $V_D$ developed across $Q_5$ and $Q_6$ bipolar devices connected as diodes operating in high-injection and taking into account the $Q_1 , Q_2 , Q_3 , Q_4$ base currents and $I_0 = \beta I_B I_B$ is given by Eq. 2.

\[
V_D = \frac{\alpha_1 I(1+x)}{\beta_1 \left(1 + e^{2VT}\right)} + \frac{\alpha_2 I(1+x)}{\beta_2 \left(1 + e^{2VT}\right)} - \frac{\alpha_3 I(1-x)}{\beta_3 \left(1 + e^{2VT}\right)} - \frac{\alpha_4 I(1-x)}{\beta_4 \left(1 + e^{2VT}\right)}
\]

The output current depends on the product of input variables x and y and also shows linear components in x and y as well as offset current. As long as the α parameter is bias dependent, biasing all bipolar transistors with same current can cancel out the opposite terms in α as indicated in Eq. 6. However, in dynamic operation the current level for a specific transistor changes and so does the α parameter for that transistor, causing an increase of non-linearity in circuit operation. Higher bias current make the parameter more sensible to current changes. Likewise, moderate variations around the operating point brings about the same effect, giving rise to a non-linearity operation of less than 1%, as will be shown in Experimental Results Session. For design purposes, an average α based on the operating point can be used for calculating the overall gain of the circuit.

4. Implemented CMOS Circuit

A CMOS implementation of the multiplier is shown in Fig. 4. The circuit makes use of input transconductors implemented with two active-loaded p-channel differential pairs. The differential mode transfer characteristic of the MOS transconductors is $1,4 I_{bias}$ [µA/V]. An output current mirror is implemented with p and n-channel transistors to output the difference current $\Delta I$. The bias current is replicated through p-channel cascode current mirrors to form the tail currents of the two MOS transconductors. The bias current ranges from 50µA to 200µA, an adequate compromise between linearity and efficiency. Efficiency is understood in this context as the ratio of the output current and tail current. The output current signal $\Delta I$ is converted into voltage through a transresistance stage. In most tests carried out,
a 50-ohm referred-to-ground resistive load along with a 2.5V floating voltage source was used as transresistance stage.

The lateral-bipolar-differential-pairs were laid out in cross-quad configuration to improve matching. The die photomicrograph of the test chip is shown in Fig. 5. The circuit dimensions are 200µm x 120µm.

The output current can be calculated from Eq. 5 and MOS transconductors gain of 1,4.IBIAS [µA/V] taking into account an average α parameter for all bipolar transistors. Therefore, the output current is given \[ \Delta I = V_{in1}V_{in2} (\Sigma \alpha) I_B/2 \] if all bipolar transistors have the same α. For a bias current of \[ I_B = 2I = 200\mu A, \alpha = 0.5, \] and applying Eq.5, \[ \Delta I = 100\mu A \] for the used transconductors and assuming a voltage input range of \[ \pm 0.5V, \] the maximum output current is \[ \Delta I = 100\mu A \pm 50\mu A. \]

5. Experimental Results

The measured frequency response is shown in Fig. 7. One input is fixed at a DC value and the other is frequency-varied. The –3 dB frequency corner is around 30MHz for 50Ω load impedance and 200µ bias current. The output noise spectral density measured on 100KΩ load resistor and amplified by a factor of 60dB gain is shown in Fig. 8. From this measurement, the output noise current spectral density for white noise is 100pA/√Hz. For lower frequencies, e.g. 100Hz, the output noise current spectral density is 300pA/√Hz. Previous reports in CMOS implementation has shown a white noise spectral density of about 300pA/√Hz [2].
The noise measurements were carried out based on a battery-fed shielded-instrumentation auxiliary circuit as shown in Fig. 9. Finally, a summary of the proposed circuit is shown in Tab I.

![Fig. 9. Measurement Setup](image)

### TABLE I

<table>
<thead>
<tr>
<th>Specs</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumption</td>
<td>50µA&lt;IBIAS&lt;200µA</td>
<td>3.1IBIAS</td>
<td>A</td>
</tr>
<tr>
<td>Average Noise (White)</td>
<td>1kHz &lt; f &lt; 10MHz @1KΩ</td>
<td>100</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Voltage Input Range</td>
<td>1.5V&lt;V_{in1},V_{in2}&lt;2.5V</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output Current Range</td>
<td>I_{max}=200µA</td>
<td>±50µ</td>
<td>A</td>
</tr>
<tr>
<td>Signal/Noise</td>
<td>V_{in}=2V_{DC}±100mV_{pk-pk} @1MHz</td>
<td>96.7</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>V_{in}=2.50 V_{DC}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_{in}=1µΩ, I_{max}=200µA</td>
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<td></td>
</tr>
<tr>
<td>THD</td>
<td>1.5V&lt;V_{in1},V_{in2}&lt;2.5V</td>
<td>&lt; 1</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>I_{max}=200µA (-3dB)</td>
<td>30</td>
<td>MHz</td>
</tr>
</tbody>
</table>

![Fig. 10 Instantaneous Switching losses of a power MOS transistor](image)

### 6. Application Envisaged

The envisaged application for this multiplier circuit relies on Smart-Power circuits, as a detector of commutation losses in power MOS transistors. This feature is suitable for integrated SMAs (Switched Mode Applications), where the power MOS and the losses detector are built together. One of the inputs of the multiplier is fed with the total voltage across the power device whereas the other one is fed with an image of the total current flowing through it. Either I-V converters can be used to read the total current before applying the correspondent signal into multiplier input or the sampled current can be input directly in differential mode into the multiplier circuit. The output information will be the instantaneous and average dissipation losses in the power MOS, that can be used as an additional protection feature. Thus, both in case of overload or switching losses excess, the main controller gets this information instantly and takes the corrective actions. A thermal or overload protection would have such a delay that can put at risk the power transistor. Fig. 10 shows the instantaneous dissipated power during the commutation intervals for an integrated power MOS switching 12V and 1A. Voltage and current dividers were used to input both signal to the multiplier circuit.

### 7. Conclusions

A Gilbert Cell-based multiplier using lateral bipolar transistor available in CMOS process is proposed. It is know that this device exhibits low $\beta$ and $\alpha$ parameters. Moreover, this device reaches high injection regime at relatively low currents. However, by adjusting the operating point of the circuit in such a way that all bipolar transistors operate at high injection, the output signal is kept linear for a relatively broad range of input signal. On the other hand, it was demonstrated that the low $\beta$ of these transistors do not affect the output current. Only the $\alpha$ parameter does. To alleviate this dependency, the bias current should be power-limited in such a way the bipolar transistor become $\alpha$ insensible. This allows for the implementation of low-distortion circuit multipliers. To validate the above mentioned, such a circuit was implemented and tested. Finally, an envisaged application as a switching losses detector for Smart-Power circuits is proposed.

### References


