MAGNETICALLY-COUPLED CURRENT SENSOR USING AN INTEGRATED COIL AND A CMOS SPLIT-DRAIN TRANSISTOR

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Abstract— An integrated current sensing circuit intended for Smart-Power and embedded applications featuring galvanic isolation is implemented. It is based on magnetic detection using the CMOS compatible Split-Drain transistor (MAGFET) that provides a very linear output current versus magnetic field. The current to be sensed flows through an integrated coil placed atop the split-drain transistor and produces a relatively strong magnetic coupling enough to cause a detectable transistor unbalance current. An integrated sensor built in 0.35µm CMOS technology presented an output conversion factor of 1500nA/A and a minimum detectable magnetic field around 1µT within 1Hz bandwidth in thermal range for 100µA transistor bias current.

Keywords— Magfet, split-drain, noise, current measurement.

1. Introduction

Current sensing is one of the most important functions to be implemented on a smart power chip and hybrid systems (Murari, 2000). In addition to providing current limitation, it is also required to detect failure situations such as short-circuit or open-load as well as to provide the feedback signal to control purposes. The classical method for current sensing is to insert a sensing resistor in the current path of power device to obtain a voltage signal that can be read by the analogue circuitry. Such a simple method has a disadvantage of introducing additional losses in the smart power circuit. Other techniques include the drain-source resistance voltage reading. The main drawback of this technique is the low accuracy due to the non-linearity of drain-source resistance. This method enjoys commercial use because of its efficiency (no additional resistor is used). Another technique was introduced in (Midya, P., et al., 2001). It uses the inductor voltage (in the case of a DC-DC PWM converter) to measure the inductor current. The approach is based on an integrator that converts voltage to current by integration over time. The main disadvantage is that the inductor value should be known exactly. Another very employed technique is based on the SENSEFET (Yuvarajan, 1990). The idea is to build a parallel MOS transistor with the main one to share a proportional load current. Since the VGS and VDS are the same, the current sharing will follow the rationed transistors areas. Despite being a practical approach, additional circuitry is necessary to follow the VDS voltage, bringing about extra complexity when the technique is applied to either high-side or low-side drivers. Moreover, the technique is reported to be both noisy and low-bandwidth (Grant and Willians, 1992). And last but not least, the SENSEFET approach does not present a galvanic isolation between power circuit and control circuitry, what can result in inconveniences in some applications. As an alternative solution, an integrated circuit application based on magnetic coupling using a split-drain transistor and an integrated coil placed on top of it and over the field silicon dioxide layer it is presented in this paper. This approach assures a real galvanic isolation because there is no electric connection between the split-drain transistor and the coil, whereof the current associated with the power or high-voltage circuit flows through. In an integrated circuit, the field silicon dioxide layer can bear about 1MV/mm allowing galvanic isolation-featured applications such as in the automotive industry, telecommunications, switched converters, household appliances and so on. As long as what is needed for measuring and controlling purposes is the image of the actual current, the integrated coil can sense the
scaled current by using a shunt element, external to the circuit and sized according the required application. Furthermore, voltage sensing can be thought as well by using a series resistor. The self-inductance of the integrated coil is very low, allowing such voltage measurements, even at high frequencies. This paper is organized as follows: In section II some basic aspects of the split-drain sensor is revised. In Section III, the 0.35µm CMOS integrated circuit is presented. Section IV addresses the thermal noise issues and associated resolution above the 1/f region. Section V shows some experimental results followed by the conclusions.

2. Split-Drain-Based Magnetic Sensor: Basics

The envisaged current sensor is based on the well-known magnetic sensor CMOS-compatible Split-Drain transistor (MAGFET) (Fry and Hoey, 1969), (Popovic, 1991). This sensor produces a current imbalance dictated by Lorentz force and can detect perpendicular magnetic field upon it, according (1).

\[ \Delta I = S I_b B \] (1)

In (1), \( \Delta I \) stand for the total current imbalance between the drain terminals of the transistor given in [Ampere], S the device sensitivity [1/T], \( I_b \) the split-drain bias current [Ampere] and B the magnetic field [T] applied perpendicularly to the device. The sensitivity depends on the device geometry (length and width) and Hall carrier mobility (\( \mu_H \)) and is related to (2).

\[ S = \mu_H G \frac{L}{W} \] (2)

For rectangular shapes in the range \( 0.85 < W/L < \infty \), the geometrical correction factor (G) is given in (3) (Popovic, 1991). For square geometries, G≈0.676.

\[ G = 1 - \frac{16}{\pi^2} e^{-\frac{\pi}{W}} \left( 1 - \frac{8}{9} e^{-\frac{\pi}{W}} \right) \] (3)

The Hall mobility (\( \mu_H \)) is given by the product of the effective carrier mobility \( \mu \) (process-based) and the Hall Factor \( r_H \). According (Jungemann et al,1999), the Hall factor for NMOS transistors is \( r_H=1.05 \) within the temperature range -20°< T <120° degrees Celsius. This value is considered to be appropriate for most practical applications. The carrier mobility parameter in the used 0.35µm CMOS process is \( \mu_H=0.037 m^2/V.S \) for NMOS transistors. The above expressions will be used in next session.

3. Implemented Current Sensor

A double metal-layer (available in the 0.35µm CMOS technology) integrated coil and the split-drain transistor whose dimensions are \( W=10\mu m \) and \( L=10\mu m \) make up the sensor circuit. The coil is placed atop the transistor to concentrate the magnetic flux lines. As the involved distances are of the micrometer order, the magnetic field intensity is enough to be detected by the split-drain transistor. Fig.1(a) illustrates schematically the positioning of the coil and the split-drain transistor, whose distances are obtained from the employed technology. Fig.1(b) shows a photomicrograph of the implemented sensor.

![Figure 1](image-url)
The NMOS split-drain transistor aspect ratio was chosen unity (L=W=10μ) so the sensitivity obtained is very close to the ideal ratio (Popovic, 1991), (Baltes, et al, 1984). By using (2) and technology parameters the calculated sensitivity is S=0.026/T. According (1) the split-drain output current depends on the bias current. Typical bias current for the split-drain can be IB=100μA, a reasonable compromise between sensitivity and power consumption, but other values can be chosen. Therefore, for this bias current and taking into account the Fc=590mT/A magnetic-field-to-coil-current ratio calculated by MAXWELL, the differential output current for the split-drain transistor magnetic sensor is approximately 1.5µA per 1A of coil current, or 1500nA/A. Obviously the coil can only carry a few milliamps of current, according the track width and process parameters. Excessive currents can speed up the electro migration effect.

4. Noise Analysis

In order to evaluate the minimum detectable current flowing through the coil or the signal-noise ratio the noise properties of the split-drain transistor should be investigated. Split-drain noise measurements suggest that there is a negative correlation between drain noise currents. Differential noise measurements, taken at both drain terminals, have shown a RMS value greater than the expected one as predicted by the classical noise model; whence it results an excess noise current from. This behavior worsens the minimum detectable magnetic field and signal-noise ratio of the sensor. This observation was already mentioned in the literature (Baltes et al, 1988), which includes thermal and 1/f noises. A new noise model was therefore developed aimed to explain this excess-noise current in thermal region (Castaldo and Reis, 2006). The proposed noise model for the split-drain transistor is illustrated in Fig.3. Three white noise current sources are employed and represented by their RMS value within 1Hz bandwidth. Two of them model the longitudinal noise current (iL) as in an ordinary transistor, each of them carrying half the total noise current, associated with the respective drain terminal. The third source models the transversal noise current (iT) that flows between drains, bringing about the observed negative noise correlation.

The longitudinal and transversal noise currents per √Hz base are given in (4), whose parameters are K=1.381x10^-23 [J/K], T the absolute temperature [K], μ the effective mobility, L and W the length and width of the split-drain transistor. The QIT is the total transistor channel charge, and can be calculated using (5) for the split-drain transistor when operating in saturation.

\[
Q = \frac{2}{3} W L C'_{ox} (V_{gs}-V_T) \tag{5}
\]

In (5), the new process parameter is C'_{ox}, the oxide capacitance per unit area. For the 0.35µm chosen CMOS process, C'_{ox}=4.54x10^-3 F/m². The threshold voltage for N-MOS transistor in same technology is V_T=0.46V. Once the longitudinal and transversal currents are known, the differential noise current (iND) produced by the split-drain transistor can be evaluated. It is worth noting that as long as the split-drain output signal is differential mode, so is the resulting noise. Starting from the noise model depicted in Fig.3, the differential RMS noise current within 1Hz bandwidth can be easily obtained and is given in (6).

\[
i_{ND} = \sqrt{2(i_L^2 + 2i_T^2)} \tag{6}
\]

Combining (1) and (6) the minimum detectable magnetic field within 1Hz bandwidth can be
evaluated. Employing the 0.35\(\mu\)m CMOS process parameters and the chosen split-drain transistor (L=W=10\(\mu\)m), it results the graphic depicted in Fig.4. Taking into account the \(F_C=590\text{mT/A}\) factor, the minimum coil current is easily determined.

\[
\Delta I = S \times I_B \times F_C \times I_{COIL} = 0.026 \times 115\mu \times 0.59 \times 0.02 = 36 \times 10^{-9}\text{A}. 
\]

This value is in good agreement with the experimental result obtained from HP4155 measurement and depicted in Fig. 5.

5. Experimental Setup and Results

The implemented split-drain transistor was biased and the coil energized with a DC current in order to provide a magnetic field to be detected by the transistor. The semiconductor parameter analyzer HP4155 was used to test this basic configuration through its sourcing features. In the test, the bias transistor was chosen \(I_B=115\mu\)A and the coil current varied from 0 to 20mA, the coil current conduction upper limit determined by its dimensions. According (1) and the coil factor (\(F_C=590\text{mT/A}\)), the detected output transistor differential current for the maximum coil current, is \(\Delta I=S \times I_B \times F_C \times I_{COIL} = 0.026 \times 115\mu \times 0.59 \times 0.02 = 36 \times 10^{-9}\text{A}\). This value is in good agreement with the experimental result obtained from HP4155 measurement and depicted in Fig. 5.

Figure 4. Minimum detectable magnetic field above the 1/f region for the 0.35\(\mu\)m CMOS L=W=10\(\mu\)m split-drain transistor as bias current function.

Figure 5. Split-Drain output current as function of \(I_{COIL}\) for \(I_B=115\mu\)A

Dynamic tests were also carried out, however an additional instrumentation circuit was employed so the signals can be better visualized. In order to convert the differential current into a differential voltage, a pair of matched low-noise resistors was used. Additionally, an instrumental amplifier was adjusted to provide a differential gain of \(G=50\), as shown in Fig. 6.

As before, the split-drain transistor was \(I_B=115\mu\)A biased and 15mA current pulses were applied to the coil. In the amplifier output 62mV-pulses were obtained, according \(V_{out}=R \times \Delta I \times G = 47 \times 10^3 \times 0.026 \times 115\mu \times 0.59 \times 0.015 \times 50 = 62\text{mV}\). This value can be verified in Fig. 7. The offset was not adjusted in this experiment. These preliminary experimental results have confirmed the predictions obtained from the calculated sensitivity analysis and from electromagnetic simulations as well.

Figure 6. Instrumental circuit associated to the basic configuration

Figure 7. Amplifier output for 15mA \(I_{COIL}\) pulses.

An AC test was also carried out. A 60Hz-current coil \(I_{COIL}=2.5\text{mA}_{\text{RMS}}\) was tested for same transistor bias conditions. Taking into account the current-to-voltage conversion gain, the output voltage will be \(V_{out}=R \times \Delta I \times G = 47 \times 10^3 \times 0.026 \times 115\mu \times 0.59 \times 2.5 \times 10^{-3} \times 50\) which gives \(V_{out} = 10.3\text{mV}_{\text{RMS}}\) or \(-39.6\text{ dBV}\) for the already mentioned parameters. Fig.8 shows the results: Bottom trace: Applied current coil; Middle: FFT of the detected output voltage; Top: Time domain output voltage.
Next, the split-drain transistor noise current is checked. To do so, a setup using two instrumental amplifiers whose gain is adjusted to 1900 (65.6dB) each one is used in conjunction with a two-channel signal analyzer HP3562A featuring cross-correlation algorithm, as shown in Fig.9(a). The cross-correlation technique eliminates the instrumental amplifier noise (Castaldo and Reis, 2006), (Ferrari and Sampietro, 2002) and gives the differential noise voltage spectral density ($\sqrt{V_{PSD}}$) whose value can be converted to current taking into account the 47kΩ I-V converter resistors. This procedure allows evaluating the measured differential noise current. This value can be checked out against the theoretical one predicted by (6). Thus, for the technology parameters and transistor bias current, the thermal noise spectral density along with the measured values within 1Hz bandwidth are given in Fig.9(b).

A current sensing technique showing galvanic isolation for integrated circuits is devised. The sensor is based on the Split-Drain transistor that can detect magnetic fields and show very linear response to the applied field. A current that is carried through an integrated metal coil generates the magnetic field. This coil is placed atop the split-drain transistor what provides strong magnetic coupling, allowing a detection ratio of 1500nA/A differential output current per sensed current. The noise analysis is necessary to evaluate the minimum detectable coil current. Furthermore, noise measurements show that this approach can be conveniently used in several integrated current sensing applications. For higher current levels, a shunt resistor can be used in order to alleviate the integrated coil and alleviate the electro migration effect.

**Conclusions**

A current sensing technique showing galvanic isolation for integrated circuits is devised. The sensor is based on the Split-Drain transistor that can detect magnetic fields and show very linear response to the applied field. A current that is carried through an integrated metal coil generates the magnetic field. This coil is placed atop the split-drain transistor what provides strong magnetic coupling, allowing a detection ratio of 1500nA/A differential output current per sensed current. The noise analysis is necessary to evaluate the minimum detectable coil current. Furthermore, noise measurements show that this approach can be conveniently used in several integrated current sensing applications. For higher current levels, a shunt resistor can be used in order to alleviate the integrated coil and alleviate the electro migration effect.

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